Amendments to the Claims

The listing of claims will replace all prior version, and listings, of claims in the application.

Listing of Claims

Claim 1 (previously presented)

A structure of nonvolatile memory array, comprising:

a substrate;

a plurality of isolation regions in said substrate;

a buried conductive region between said plurality of isolation regions, wherein said buried conductive region is perpendicular to each of said plurality of isolation regions; and

a plurality of gate structures on said substrate except not on said buried conductive region.

Claim 2 (currently amended)

The structure according to claim 1, wherein each of said plurality of isolation regions ~~is shallow~~ is a shallow trench isolation.

Claim 3 (original)

The structure according to claim 1, wherein a depth of said buried conductive region is less than a depth of said isolation region.

Claim 4 (previously presented)

The structure according to claim 1, wherein each of said plurality of gate structures comprises at least a polysilicon layer.

Claim 5 (previously presented)

The structure according to claim 1, further comprising a plurality of contacts on said substrate.

Claim 6 (original)

The structure according to claim 1, wherein said buried conductive region is a source line.

Claim 7 (previously presented)

The structure according to claim 1, further comprising a plurality of drain regions in said substrate.

Claim 8 (previously presented)

The structure according to claim 1, wherein said buried conductive region is on a surface of said substrate, such that said buried conductive region is not under said plurality of isolation regions.

Claim 9 (previously presented)

A structure of nonvolatile memory array, comprising:

a substrate;

a plurality of isolation regions in said substrate;

a plurality of gate structures on said substrate;

a buried source line between said plurality of isolation regions, wherein said buried source line is perpendicular to each of said plurality of isolation regions, and wherein the gate structures are not positioned on said buried source line; and

a plurality of drain regions in said substrate.

Claim 10 (previously presented)

The structure according to claim 9, wherein each of said plurality of isolation regions is shallow trench isolation.

Claim 11 (previously presented)

The structure according to claim 9, wherein a depth of said buried source line is less than a depth of said plurality of isolation regions.

Claim 12 (previously presented)

The structure according to claim 9, wherein each of said plurality of gate structures comprises at least a polysilicon layer.

Claim 13 (previously presented)

The structure according to claim 9, further comprising a plurality of contacts in said substrate.

Claims 14-20 (Canceled)

Claim 21 (New)

A structure of nonvolatile memory array, comprising:

a substrate;

a plurality of isolation regions in said substrate;

a plurality of gate structures on said substrate;

a buried source line between said plurality of isolation regions, wherein said buried source line is perpendicular to each of said plurality of isolation regions and a depth of said buried source line is less than a depth of said plurality of isolation regions, and wherein the gate structures are not positioned on said buried source line; and

a plurality of drain regions in said substrate.

Claim 22 (New)

The structure according to claim 14, wherein each of said plurality of isolation regions is a shallow trench isolation.

Claim 23 (New)

The structure according to claim 14, wherein each said plurality of gate structures comprises at least a polysilicon layer.

Claim 24 (New)

The structure according to claim 14, further comprising a plurality of contacts in said substrate.